What is claimed is:

1. A delay locked loop (DLL) circuit, comprising:

a clock buffer for receiving an external clock signal, temporarily storing the external clock signal and outputting a buffered clock signal;

a first frequency divider for receiving the buffered clock signal and generating a divided clock signal by dividing the buffered clock signal according to a dividing control signal;

a phase detector for receiving the divided clock signal from the first frequency divider and the buffered signal from the clock buffer, detecting phase delay of two signals, generating a first comparison signal and a second comparison signal and generating a sample clock signal in order to perform sampling of the second comparison signal;

a DLL controller for receiving and analyzing the sample clock signal and the second comparison signal from the phase detector, and outputting a dividing control signal as a second logic level when an analyzing result is an high speed operation or outputting a dividing control signal as a first logic level when an analyzing result is an low speed operation;

a delay line for receiving the buffered clock signal from the clock buffer and the first comparison signal and the second comparison signal from the phase detector, performing shifting of the external clock signal to the left or right

according to the first comparison signal and the second comparison signal, and outputting an internal clock signal;

a second frequency divider for receiving the internal clock signal from the delay line and generating a divided internal signal by dividing the internal clock signal according to the dividing control signal; and

a replica unit for receiving the divided internal signal from the second frequency divider, compensating the time delay between the external clock and the internal clock and generating the compensation clock signal.

2. The DLL circuit as recited in claim 1, wherein the DLL controller includes:

a divider including a plurality of RT flip-flops for receiving the buffered clock signal from the clock buffer and a reset signal from an external part and generating a divided clock signal by dividing the buffered clock signal;

a synchronizing unit including a plurality of FD flip-flops for receiving the buffered clock signal from the clock buffer, a plurality of the divided clock signals from the divider and a reset signal from an external part, synchronizing the divided clock signals at falling edge of the buffered clock signal and generating a plurality of the synchronized clock signals;

a DLL enable signal generating unit for receiving a plurality of synchronized clock signals and reversed signals of the synchronized clock signals, generating a plurality of

enable signals and a dividing cycle signal and controlling enable of the DLL circuit according to the enable signals; and

a dividing controller for receiving the dividing cycle signal from the DLL enable signal generating unit, the sample clock signal and the second comparison signal from the phase detector, a reset signal and a test mode signal, performing sampling of the second comparison signal according to the sample clock signal, analyzing the second comparison signal and the sample clock signal in order to determine the operation speed and outputting the dividing control signal as the second logic level for the high speed operation or outputting the dividing control signal at the first logic level for the low speed operation.

3. The DLL circuit as recited in claim 2, wherein the test mode signal is used to control the dividing control signal during test.

4. The DLL circuit as recited in claim 2, wherein the DLL enable signal generating unit includes:

a first inverter for reversing a received reset signal and outputting a reversed reset signal;

a first NAND gate for receiving the second synchronized clock signal among a plurality of the synchronized clock signals and the reversed signals of the synchronized clock signals and performing a NAND operation;

a second NAND gate which is cross-coupled with the first

NAND gate for receiving the reversed reset signal and performing a NAND operation;

a second inverter for receiving the output signal from the second NAND gate and reversing the output signal of the second NAND gate;

a third inverter for receiving the output signal from the second inverter, reversing the output signal and outputting a reversed signal of a first enable signal among a plurality of the enable signals;

a forth inverter for receiving the reversed signal of a first enable signal and reversing the reversed signal of a first enable signal;

a third NAND gate for receiving the reversed signal of the first synchronized clock signal and the reversed signal of the second synchronized clock signal among a plurality of the synchronized clock signals and the reversed signals of the synchronized clock signals and performing a NAND operation;

a forth NAND gate for receiving the reversed signal of the third synchronized clock signal and the reversed signal of the forth synchronized clock signal among a plurality of the synchronized clock signals and the reversed signals of the synchronized clock signals and performing a NAND operation;

a NOR gate for receiving the output signals from the third NAND gate and the forth NAND gate and performing a NOR operation;

a fifth NAND gate for receiving the output signal from the NOR gate and performing a NAND operation;

a sixth NAND gate for receiving the reversed reset signal and the output signal of the fifth NAND gate and performing a NAND operation;

a fifth inverter for receiving the output signal from the sixth NAND gate and reversing the output signal;

a seventh NAND gate for receiving the third synchronized clock signal among a plurality of the synchronized clock signals and the reversed signals of the synchronized clock signals and performing a NAND operation;

an eighth NAND gate which is cross-coupled with the seventh NAND gate for receiving the output signal from the fifth inverter and performing a NAND operation;

a ninth NAND gate for receiving the forth synchronized clock signal among a plurality of the synchronized clock signals and the reversed signals of the synchronized clock signals and performing a NAND operation;

a tenth NAND gate which is cross-coupled with the ninth NAND gate for receiving the reversed reset signal and performing a NAND operation;

an eleventh NAND gate for receiving the output signals of the eighth NAND gate and the tenth NAND gate and performing a NAND operation;

a sixth inverter for receiving the output signal from the eleventh NAND gate and reversing the output signal of the eleventh NAND gate;

a seventh inverter for receiving the output signal of the sixth inverter and reversing the output signal of the sixth

inverter;

an eighth inverter for receiving the output signal from the seventh inverter and reversing the output signal from the seventh inverter;

a ninth inverter for receiving the output signal from the eighth inverter and reversing the output signal of the eighth inverter;

a tenth inverter for receiving the output signal from the ninth inverter and reversing the output signal of the ninth inverter;

a first delay unit for receiving the output signal from the tenth inverter and delaying the output signal from the tenth inverter;

an eleventh inverter for receiving the output signal from the first delay unit and reversing the output signal from the first delay unit;

a twelfth NAND gate for receiving the output signal of the eleventh inverter and the first enable signal and performing a NAND operation;

a twelfth inverter for receiving the output signal from the twelfth NAND gate and reversing the output signal of the twelfth NAND gate;

a 13^{th} inverter for receiving an output signal of the tenth NAND gate and reversing the output signal of the tenth NAND gate;

a 14^{th} inverter for receiving an output signal of the 13^{th} inverter and reversing the output signal of the 13^{th} inverter;

a 13th NAND gate for receiving output signals of the twelfth inverter and the 14th inverter and performing a NAND operation;

a 15th inverter for receiving an output signal of the 13th NAND gate and reversing the output signal of the 13th NAND gate;

a 16th inverter for receiving an output signal of the 15th inverter and reversing the output signal of the 15th inverter;

a 17th inverter for receiving an output signal of the 16th inverter and reversing the output signal of the 16th inverter; and

a 18th inverter for receiving an output signal of the 14th inverter and reversing the output signal of the 14th inverter.

5. The DLL circuit as recited in claim 2, wherein the dividing controller includes:

a 19th inverter for receiving the dividing cycle signal and reversing the dividing cycle signal;

a 20th inverter for receiving an output signal of the 19th inverter and reversing the output signal of the 19th inverter;

a second delay unit for receiving an output signal of the 20th inverter and delaying the output signal of the 20th inverter;

a 14th NAND gate for receiving an output signal of the second delay unit and an output signal of the 20th inverter and performing a NAND operation;

a 15th NAND gate for receiving the output signal of the

20th inverter and the second comparison signal and performs a NAND operation;

a 21st inverter for receiving an output signal of the 15th NAND gate and reversing the output signal of the 15th NAND gate;

a 22nd inverter for receiving the sample clock signal and reversing the sample clock signal;

a 23rd inverter for receiving an output signal of the 22nd inverter and reversing the output signal of the 22nd inverter;

a 24th inverter for receiving an output signal of the 23rd inverter and reversing the output signal of the 23rd inverter;

a 25th inverter for receiving an output signal of the 24th inverter and reversing the output signal of the 24th inverter;

a first PMOS transistor, wherein a source of the first PMOS transistor is coupled to a power unit and a gate of the first PMOS transistor receives an output signal of the 14th NAND gate;

a first NMOS transistor, wherein a drain of the first NMOS transistor is coupled to a drain of the first PMOS transistor and a gate of the first NMOS transistor receives an output signal of the 21st inverter;

a second NMOS transistor, wherein a drain of a second NMOS transistor is coupled to a source of the first NMOS transistor, a source of the second NMOS transistor is grounded and a gate of the second NMOS transistor receives an output signal of the 25th inverter;

a 26th inverter for receiving the reset signal and

reversing the reset signal;

a second PMOS transistor, wherein a source of the second PMOS transistor is coupled to a power, a gate of the second PMOS transistor receives an output signal of the 26th inverter and a drain of the second PMOS transistor is coupled to the drain of the first PMOS transistor;

a 27th inverter for receiving a signal from the drain of the first PMOS transistor and reversing the signal from the drain of the first PMOS transistor;

a 28th inverter for receiving an output signal of the 27th inverter and reversing the output signal of the 27th inverter;

a 29th inverter for receiving an output signal of the 27th inverter and reversing the output signal of the 27th inverter;

a third NMOS transistor, wherein a gate of the third NMOS transistor receives the test mode signal, a drain and a source of the third NMOS transistor are common-grounded and operating as a capacitor;

a forth NMOS transistor, wherein a drain of the forth NMOS transistor receives the test mode signal and a source of the forth NMOS transistor is grounded;

a 30th inverter for receiving the test mode signal and reversing the test mode signal;

a 16th NAND gate for receiving an output signal of the 29th inverter and an output signal of the 30th inverter and performing a NAND operation;

a 31st inverter for receiving an output signal of the 16th NAND gate and reversing the output signal of the 16th NAND

gate; and

a 32nd inverter for receiving an output signal of the inverter and reversing the output signal of the inverter.